ABSTRACT

0038 A CMOS structure including a Slim spacer and method for forming the same to reduce an S/D electrical resistance and improve charge mobility in a channel region, the method including providing a semiconductor substrate including a polysilicon gate structure including at least one overlying hardmask layer; forming spacers selected from the group consisting of oxide/nitride and oxide/nitride oxide layers adjacent the polysilicon gate structure; removing the at least one overlying hardmask layer to expose the polysilicon gate structure; carrying out an ion implant process; carrying out at least one of a wet and dry etching process to reduce the width of the spacers; and, forming at least one dielectric layer over the polysilicon gate structure and spacers in one of tensile and compressive stress.